REMARKS

Claims 45, 46, 50-52, 54-56, 59, 60, 68-70, 73, 74 and 77 are pending in this application. Claims 51, 52, 68 and 73 have been amended. No new matter has been introduced. As suggested in the last Office Action, claims 51 and 52 have been rewritten in independent form to include all limitations of independent claim 68 and are now in condition for allowance.

Claims 54-56, 59, 60, 73 and 74 stand rejected under 35 U.S.C. § 112, second paragraph, on the basis that the term "increased" doping concentration in claim 73 is unclear. (Office Action at 2). Independent claim 73 has been amended to recite that "said increased doping concentration [is] higher than a doping concentration of said first area" correcting, therefore, any perceived indefiniteness. Applicant respectfully submits that all pending claims are now in full compliance with 35 U.S.C. § 112.

Claims 45, 46, 50, 54-56, 68-70, 73, 74 and 77 stand rejected under 35 U.S.C. § 103 as being unpatentable over Schuegraf et al. (U.S. Patent No. 5,702,976) ("Schuegraf") in view of Kooi et al. (U.S. Patent No. 3,755,001) ("Kooi") and Joo et al. (U.S. Patent No. 5,841,163) ("Joo"). This rejection is respectfully traversed.

The claimed invention relates to isolation trenches formed of two dielectric materials. As such, amended independent claims 68 and 73 recite an integrated circuit and a memory device, respectively, comprising "a field isolation region" separating a plurality of active regions and including "an isolation trench." Amended independent claims 68 and 73 further recite that the isolation trench includes "a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls." Amended independent claim 68 also recites "a doped region . . . below said second area, said doped region . . . having a doping concentration higher than a doping concentration of said first region, wherein additional dopants in said doped region causing said higher doping concentration are displaced away from said separated active regions."

Amended independent claim 73 also recites "an ion implanted region provided below said second area having an increased doping concentration in an area of said substrate between said separated active regions, said increased doping concentration being higher than a doping concentration of said first area." Amended independent claim 73 further recites that "substantially all ions from said ion implanted region which increase said doping concentration are displaced away from said active regions by a distance at least equal to a sidewall thickness of said first area filled with said first dielectric material."

Schuegraf relates to "a trench isolation process which alleviates the problem of void formation during dielectric refill." (Col. 2, lines 49-51). According to Schuegraf, "recesses (22) preferably having a trench profile" are formed by removing portions of a semiconductor substrate 10. (Col. 2, lines 60-61; Figure 3A). Schuegraf teaches that "[t]he trenches (22) are then refilled with a material (26) having a dielectric constant lower than the dielectric constant of silicon dioxide." (Col. 2, lines 61-63; Figure 3D). To avoid contamination of substrate regions adjacent to trenches 22, Schuegraf further teaches that "it is preferable to form a barrier layer 24 over the trenches 22 prior to dielectric refill." (Col. 5, lines 9-12; Figure 3B). In this manner, by "utilizing dielectric materials having a lower dielectric constant that used in the prior art," the shallow trench isolation of Schuegraf "maintains effective device isolation." (Col. 4, lines 37-40).

Kooi relates to a method of fabricating semiconductor devices having selective doping and selective oxidation. (Title; Col. 1, lines 4-11). As part of the fabrication of "a target plate (1) for converting electromagnetic radiation into electric signals," Kooi teaches that grooves 4 formed into plate 1 of n-type silicon "are covered with a layer 5 of silicon oxide which at the bottom of the grooves adjoins a surface zone 6 of n-type silicon having higher doping that the region 1." (Col. 6, lines 9-20; Figures 1-2).

Joo relates to integrated circuit structures having wide and narrow channel stop layers which are formed by employing a first and second field insulation layers coupled with a first and second channel stop impurity layers. (Col. 3, lines 38-47). For example, Joo discloses that impurity ions are implanted below the first field oxide layer and are diffused

by a thermal process to form a second channel stop impurity layer. (Col. 6, lines 36-50; Figure 15).

The subject matter of claims 45, 46, 50, 54-56, 68-70, 73, 74 and 77 would not have been obvious over Schuegraf in view of Kooi and Joo. Indeed, the Office Action fails to establish all elements of a showing of a *prima facie* case of obviousness. Specifically, the prior art references fail to teach or suggest all claim limitations. None of Schuegraf, Kooi and Joo teaches or suggest trenches separating "a plurality of active regions" and having a first and a second areas filled with corresponding dielectric materials and "a doped region within said first region below said second area, said doped region . . . having a doping concentration higher than a doping concentration of said first region, wherein *additional dopants in said doped region . . . are displaced away from said separated active regions*," as amended independent claim 68 recites (emphasis added). None of Schuegraf, Kooi and Joo teaches or suggest trenches separating "a plurality of doped active regions" and having a first and a second areas filled with corresponding dielectric materials as well as "an ion implanted region . . . below said second area . . . *substantially all ions from said ion implanted region . . . displaced away from said active regions*," as amended independent claim 73 recites (emphasis added).

Schuegraf discloses trenches which are "refilled with a dielectric material" with low dielectric constant and which may be lined with a barrier layer 24 prior to the dielectric refill. (Col. 3, lines 61-62). However, Schuegraf does not teach or suggest an ion implanted region directly below the second dielectric area, as in the claimed invention. Schuegraf is also silent about any ions from an ion implanted region "being displaced away from" the active regions, as independent claims 68 and 73 recite. In fact, Schuegraf does not even mention the existence of active regions in the "Detailed Description," or illustrate any such active regions in the "Drawings."

Kooi also does not disclose an isolation trench or "a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls," as amended independent

claims 68 and 73 recite. Further, Kooi does not disclose "a doped region" (claim 68) or "an ion implanted region" (claim 73) located "below said second area," as amended independent claims 68 and 73 recite. Kooi is also silent about the ion displacement limitations of claims 68 and 73. As shown in Figures 8 and 10 of Kooi, the ion implanted regions 6 and 28 are in contact with the dielectric materials 5 and 29, respectively, but these dielectric materials are simply not part of an isolation trench.

Joo also fails to disclose an isolation trench, much less first and second areas filled with first and second dielectric materials, or an ion implanted region below the second area, or that substantially all ions in the implanted region are displaced away from the separated active regions, as amended independent claims 68 and 73 recite. Joo teaches a "first channel stop impurity layer 67" formed beneath the second field oxide layer 66 and "a second channel stop impurity layer 68 beneath the first field oxide layer 65." (Col. 6, lines 1-3; 35-37; Figure 15). In Joo, however, the first and second channel stop impurity layers and the first and second field oxide layers are not part of an isolation trench, much less of an isolation trench filled with first and second dielectric materials, as in the claimed invention.

Shuegraf, Joo and Kooi, considered alone or in combination, also fail to teach or suggest "an isolation trench having a depth of about 3,500 Angstroms . . . including a first area filled with a first dielectric material . . . and a second area filled with a second dielectric material," as amended independent claim 68 recites. In fact, Schuegraf teaches away from the subject matter of amended independent claim 68 by specifically emphasizing that "the trenches of [Schuegraf] are about 200 nm deep, shallower than the prior art by about 20%." (Col. 5, lines 6-8). Further, Kooi and Joo are silent about any trench dimensions, much less about isolation trenches "having a depth of about 3,500 Angstroms . . . including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls, wherein said first dielectric material and said second dielectric material are different," as in the claimed invention.

A marked-up version of the changes made to the claims by the current amendment is attached. The attached page is captioned "**Version with markings to show changes made.**"

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

51. (Twice Amended) [The integrated circuit of claim 68] An integrated circuit comprising:

a semiconductor substrate including a first region of a predefined conductivity type;

a plurality of active regions provided within said first region;

a field isolation region separating at least two of said active regions, wherein said field isolation region includes an isolation trench, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls, wherein said first dielectric material and said second dielectric material are different; and

a doped region within said first region below said second area, said doped region being of said predefined conductivity type and having a doping concentration higher than a doping concentration of said first region, wherein additional dopants in said doped region causing said higher doping concentration are displaced away from said separated active regions and wherein said additional dopants are implanted into the substrate below said first area filled with said first dielectric material to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material.

52. (Twice Amended) [The integrated circuit of claim 68] An integrated circuit comprising:

a semiconductor substrate including a first region of a predefined conductivity type;

a plurality of active regions provided within said first region;

a field isolation region separating at least two of said active regions, wherein said field isolation region includes an isolation trench, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls, wherein said first dielectric material and said second dielectric material are different; and

a doped region within said first region below said second area, said doped region being of said predefined conductivity type and having a doping concentration higher than a doping concentration of said first region, wherein additional dopants in said doped region causing said higher doping concentration are displaced away from said separated active regions and wherein said additional dopants are implanted into the substrate below said first area filled with said first dielectric material to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material.

68. (Twice Amended) An integrated circuit comprising:

a semiconductor substrate including a first region of a predefined conductivity type;

a plurality of active regions provided within said first region;

a field isolation region separating at least two of said active regions, wherein said field isolation region includes an isolation trench having a depth of about 3500 Angstroms, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls, wherein said first dielectric material and said second dielectric material are different; and

a doped region within said first region below said second area, said doped region being of said predefined conductivity type and having a doping concentration higher than a doping concentration of said first region, wherein additional dopants in said doped region

causing said higher doping concentration are displaced away from said separated active regions.

73. (Twice Amended) A memory device comprising:

a semiconductor substrate including a plurality of doped active regions;

a field isolation region separating at least two of said active regions, said field isolation region including an isolation trench, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls, said first dielectric material being different than said second dielectric material; and

an ion implanted region provided below said second area having an increased doping concentration in an area of said substrate between said separated active regions, said increased doping concentration being higher than a doping concentration of said first area, wherein substantially all ions from said ion implanted region which increase said doping concentration are displaced away from said active regions by a distance at least equal to a sidewall thickness of said first area filled with said first dielectric material.